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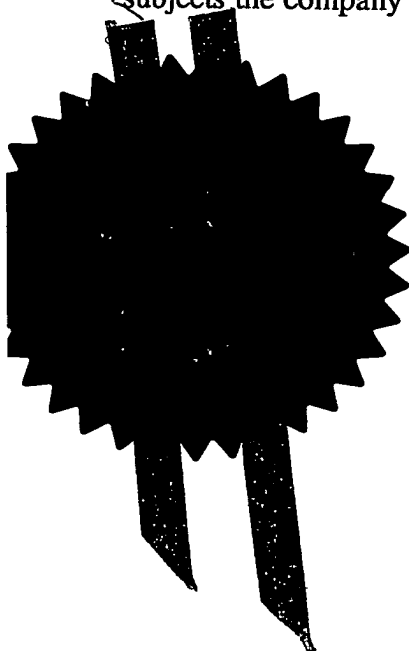
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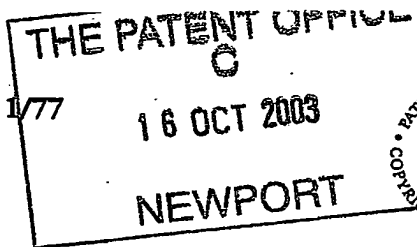
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8206484006

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SHORT-CHANNEL TRANSISTORS

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01223 765867

louise.douglas@rtd.cam.ac.uk

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Short-channel transistors

Fast speed integrated circuits require patterning techniques that is capable of defining critical features down to sub-micrometer or even nanometer scale resolution. However, in conventionally designed submicrometer transistor structures, the performance of the transistor is degraded due to the increasing off-current resulted from short channel effects. For a given thickness of the gate dielectric the gate electrode gradually loses its function to turn on/off the transistor channel with decreasing channel length or increasing source-drain voltage. Techniques for reducing the short channel effect and enabling further dimension downscaling are required.

According to one aspect of the present invention the off-current of short channel, submicrometer transistors can be greatly suppressed by inserting an insulating mesa-like barrier in-between source and drain electrodes that is coated with the semiconducting layer. The presence of the mesa which prevents current flow along the path of shortest distance between source and drain electrodes has been found to result in lowering of transistor OFF currents, while in conventional structures without mesa a high OFF current is flowing between source and drain electrodes if the channel length is below 1 μm . The beneficial role of the insulating barrier has been observed for both inorganic metal electrodes patterned by electron beam lithography, as well as conducting polymer electrodes fabricated by inkjet printing and dewetting.

The invention will now be described with reference to the following figures:

Fig.1. Comparison of conventional structure according to the prior art and mesa-structure transistors according to the present invention. (a) Conventional transistor structure and AFM picture of patterned source and drain electrodes with channel length of 400 nm and width of 200 μm . (b) mesa-structure with insulating barrier and AFM picture of patterned source and drain electrodes separated by a 50 nm high insulating barrier with channel length of 400 nm and width of 200 μm . (c, d) Transfer characteristics of a conventional structure transistor and a mesa structure transistor.

Fig. 2. Schematic diagrams of dewetting process (a) FDTS SAM is elevated by SiO_2 mesa patterned on $\text{SiO}_2/\text{n}^+\text{-Si}$ substrate. (b) PEDOT/PSS water solution is ink-jetted on top of FDTS SAM. (c) PEDOT/PSS is dewetted by FDTS / SiO_2 mesa. (d) Structure of polymer transistor fabricated by dewetting.

Fig.3. Transfer characteristics of a conventional (a and c) and a mesa structure (b and d) transistor fabricated by dewetting. Channel length for both is 500 nm, width is 80 μm .

Fig.4. Photographs of various dewetted PEDOT/PSS illustrating factors affecting dewetting . (a) PEDOT 1:1, 700 nm FDTS SAM. (b) PEDOT 1:1 , 500 nm FDTS SAM, Oxygen plasma treated surface (c) PEDOT 1:1, 300 nm FDTS SAM. (d) PEDOT 1:3, 250 nm FDTS SAM. (e) PEDOT 1:1, 500 nm FDTS SAM, 30 nm SiO_2 mesa. (f) 5 μm FDTS SAM gap, dip coated by PEDOT 1:3. (g) PEDOT 1:1 lines printed with a jet frequency of 4Hz, printing speed of 0.1 and 0.3 mm/s, 500 nm FDTS SAM, 30 nm mesa. (h) PEDOT 1:1 lines printed with a jet frequency of 4 Hz, printing speed of 0.1 and 0.3 mm/s, 500 nm FDTS SAM, 80 nm mesa.

Fig. 5 Schematic diagram of dewetting model.

Fig. 6 AFM pictures of dewetted PEDOT/PSS. Fig. 6a, b and fig. 6e show AFM topography, phase and cross-sectional images, respectively, of dewetted 1:3 PEDOT/PSS droplets split on top of a 250 nm FDTS SAM without mesa. Fig. 6c, d and f give the corresponding dewetting results of 1:1 PEDOT/PSS droplets on a 500 nm wide FDTS SAM with 30 nm mesa.

The electrode patterning process is as follows: patterning wells with trapezoidal shape (larger width on top) were written into a 250 nm resist layer of polymethylmethacrylate (PMMA) on a $\text{SiO}_2/\text{n}^+\text{-Si}$ substrate with the help of electron beam lithography. The well (or line) width was controlled by varying the exposure dose. (We used a $\text{SiO}_2/\text{n}^+\text{-Si}$ substrate to avoid charging effects.) After the development of the exposed PMMA resist the substrate surface in the electron beam exposed regions was modified with a layer of Al deposited by vacuum evaporation. Alternatively, a 50 nm thick layer of SiO_2 was sputter deposited into the narrow wells

defined by the electron beam, followed by Al deposition. Subsequently, the resist is dissolved in acetone, lifting-off the layer of Al/SiO₂ on top of the PMMA, leaving Al/SiO₂ narrow lines on the substrate, then Cr (2 nm) /Au (10 nm) stripes were evaporated crossing the Al/SiO₂ narrow lines. After removing Al by common photoresist developer MF 319 helped by ultrasonic, the structures designed as Fig. 1 were obtained. The AFM pictures of none-mesa and mesa structure are shown in Fig. 1 (both have a channel length of 400 nm). It is seen that the source and drain electrodes are separated by the mesa (Fig. 1b). After patterning source and drain electrodes, top-gate polymer FETs were fabricated by spin coating a 50 nm polymer semiconductor layer of poly(9,9'-dioctyl-fluorene-co-bithiophene) (F8T2) from xylene solution and 1 μ m insulating layer of PMMA from n-butyl acetate solution, and inkjet printing a PEDOT/PSS top gate electrode.

We have found that the use of mesa structure can dramatically decrease the off current and improve transistor performance compared to a conventional transistor with the same channel length but no SiO₂ mesa structure between source and drain electrodes. Fig. 1c shows the transfer characteristics of a conventional transistor and Fig. 1d shows the result of a mesa-structure transistor. Both transistors have a channel length of 400 nm and width of 200 μ m. It is seen that at a drain-source voltage of -10 V, both transistor exhibit good ON-OFF current ratio, although the conventional transistor has a larger current at zero gate voltage. However, for a drain-source voltage of -50 V the gate almost loses its control of the transistor current in the conventional structure. For the mesa-structure transistor it is seen that the on-off ratio remains at 10³.

Without wanting to be bound by theory, the origin of this beneficial increase of the ON-OFF current ration in submicron transistor by use of an insulating mesa is believed to related to the mesa blocking the direct conduction path between source and drain. In contrast in the conventional structure current can directly flow from source to drain. Detailed device modeling is currently being performed to investigate this. Another possible factor that could be responsible for the effect of the mesa structure is the blocking by the mesa of impurities from the glass substrate to come in direct contact with the semiconducting layer. The mesa might prevent interfacial

doping that occur when the semiconducting layer comes in direct contact with the substrate, that might contain ionic impurities such as sodium, that might be able to induce doping of the semiconducting material.

Remarkably, we have observed similar behaviour for conducting polymer poly(3,4-ethylenedioxythiophene)/poly(4-styrenesulfonate) (PEDOT/PSS) electrodes patterned by inkjet printing and dewetting. The process is shown in Fig. 2 which is similar with the above process for patterning gold electrodes. Hydrophobic lines with widths varying from 250 nm to 20 μm were defined by electron beam lithography (EBL) (250 nm – 1 μm) and optical lithography (2-20 μm), respectively. For EBL patterning lines were written into a 250 nm resist layer PMMA on a $\text{SiO}_2/\text{n}^+\text{-Si}$ substrate. The line width was controlled by varying the exposure dose. After the development of the exposed PMMA resist the substrate surface in the electron beam exposed regions was modified with a monolayer of 1H, 1H, 2H, 2H-perfluorodecyltrichlorosilane (FDTS, $\text{C}_{10}\text{F}_{17}\text{H}_4\text{SiCl}_3$) deposited from the vapor phase. Alternatively, a 30-80 nm thick layer of SiO_2 was sputter deposited into the narrow wells defined by the electron, followed by FDTS SAM deposition. In both cases prior to the FDTS deposition the substrate surface is cleaned and conditioned by a short 2 min oxygen plasma exposure. This allowed defining mesa-structures in which the surface energy barriers have a finite thickness. Subsequently, the resist is dissolved in acetone, lifting-off the layer of FDTS/ SiO_2 on top of the PMMA and uncovering the underlying hydrophilic area of the substrate (Fig. 2a). Dewetting is then realized by ink-jetting PEDOT/PSS water droplets of different concentrations with a droplet volume of ~ 65 pl per drop on top of the patterned surface (Fig. 2b). (A 1:1 (1:3) PEDOT/PSS ink denotes a 1:1 (1:3) mixture of Baytron P PEDOT/PSS solution from Bayer and pure water.) Droplets that land on top of the narrow FDTS modified lines split into two during the drying of the ink, so defining the source and drain electrodes of the FET (Fig. 2c). Top-gate polymer FETs were fabricated employing dewetted PEDOT/PSS source and drain electrodes by spin coating a 50 nm polymer semiconductor layer of poly(9,9'-dioctyl-fluorene-co-bithiophene) (F8T2) from xylene solution and 1 μm insulating layer of PMMA from n-butyl acetate solution, and inkjet printing a PEDOT/PSS top gate electrode (Fig. 2d).

Fig. 3 c and d respectively shows transfer characteristics of a conventional structure (monolayer barrier) and mesa structure (30 nm mesa) transistor fabricated by dewetting, respectively. Both have a channel length of 500 nm and width of 80 μm . it is clearly seen that a mesa greatly improves the transistor performance, similarly to the improved performance enhancement in the case of gold electrodes.

In the following we describe in more detail the process for dewetting which is used for the fabrication of the conducting polymer electrodes.

The application of solution-based direct printing techniques to the deposition and direct-write patterning of functional materials is providing new opportunities for the manufacturing of electronic devices, such as organic field effect transistors (FETs) for applications in low-cost, large-area electronics on flexible substrates^{1,2,3,4}. A range of direct printing techniques, such as screen printing^{1,2} or inkjet printing^{3,4} has been used. However, the ability of most direct printing techniques to define micrometer-size patterns is limited to typically 20-50 μm due to the difficulties of controlling the flow and spreading of liquid inks on surfaces. One approach to overcome these resolution limitations is to deposit the functional ink onto a substrate containing a predefined surface energy pattern that is able to steer the deposited ink droplets into place. This concept has been used successfully for patterning of source-drain electrodes of polymer FETs with channel lengths of 5 μm by inkjet printing⁴. Dewetting by dip coating has also been used to pattern the active semiconducting layer in transistor fabrication^{5,6}.

The performance of FET devices would greatly benefit from further reduction of channel length to submicrometer dimensions. However, to achieve this a detailed understanding of the various factors that govern the interaction of droplets containing a solute of functional material with a patterned surface is required. Interactions between non-solute containing liquids and structured flat solid surfaces composed of hydrophilic and hydrophobic areas have been studied extensively theoretically and experimentally^{7,8,9,10,11,12,13,14}. However, no detailed investigation has been done on dewetting of solute-containing inks where the process of drying leads to an increase

of ink viscosity that limits the ability of the ink to dewet from narrow hydrophobic strips.

We investigate dewetting of PEDOT/PSS inks on patterned SiO_2 surfaces modified with the fluorinated FDTS SAM (Various hydrophobic SAMs have been widely investigated and used for their hydrophobicity^{15, 16, 17, 18}). Several factors have been found to be important to achieve splitting of droplets by submicrometer hydrophobic lines (Fig. 4). Fig. 4a and b compare dewetting of a 1:1 PEDOT ink on top of substrates with different degree of hydrophilicity in the bare SiO_2 regions. On a substrate cleaned by oxygen plasma cleaning prior to deposition of the PMMA resist, dewetting from a 500 nm wide line is observed (Fig. 4b). In contrast, if the substrate is only cleaned by washing in acetone and isopropanol, resulting in a higher contact angle and smaller droplet diameter (Fig. 4a), even on a 700 nm wide line no complete dewetting is observed. This indicates that dewetting is favoured by a low contact angle in the wetting region of the substrate. Dewetting also depends on the relative position of the center of the droplet with respect to the hydrophobic barrier. If the hydrophobic line is close to the edge of the droplet, dewetting is possible even from very narrow hydrophobic lines (compare Fig. 4a and c). Another key factor is the ink concentration and ink viscosity. Lower PEDOT/PSS concentrations enable dewetting on very narrow (250 nm) lines from which dewetting of more concentrated solutions is not possible (compare Fig. 4a and d). Finally, the use of a mesa of finite thickness also improves the ability to dewet significantly. On top of a 30 nm thick mesa a concentrated 1:1 PEDOT/PSS solution is capable of dewetting from significantly narrower lines than on top of monolayer surface energy barriers (compare Fig. 4e and a).

Finally, we have also investigated the influence of the total amount of liquid deposited by printing continuous lines of PEDOT/PSS across an array of hydrophobic FDTS stripes. The total deposited liquid volume per unit length of the line was controlled by the speed of the sample stage, while keeping the droplet ejection frequency (4Hz) the same. Fig. 4g shows dewetting result on 30 nm FDTS/ SiO_2 mesa. When the stage moves with a speed of 0.3mm/s, PEDOT/PSS solution is dewetted, whereas for a stage speed of 0.1mm/s, complete dewetting did not occur. Note that also here thicker

mesa structures promote dewetting (compare lines printed with 0.1 mm/s in Fig. 4g and h).

The fluid dynamical processes behind these observations can be rationalized by a simple model. Fig.5 shows a schematic diagram of the dewetting process (for simplicity, a two-dimensional model is used). The whole surface is covered by a thin liquid film of thickness H on top of a hydrophobic strip of length L . After dewetting, the liquid-vapor interface area is increased by an amount $(2\Delta S - L)$, where $2\Delta S$ is the increase of the surface area in the hydrophilic regions due to the curved edges on both sides of the hydrophobic strip. The liquid-solid interface area decreases by L , and the solid-vapor interface area increases by L . For the total surface/interface energy after dewetting to be less than the surface/interface energy before dewetting, the following relationship must be satisfied :

$$(2\Delta S - L)E_{LV} + (-LE_{LS}) + LE_{SV} \leq 0 \quad (1)$$

E_{LV} , E_{LS} , E_{SV} are the liquid-vapor, liquid-solid, solid-vapor interface tension respectively. Two conditions are assumed in our model: (a) The liquid volume before and after dewetting is assumed constant. (b) Gravity is neglected. Based on formula (1), complete dewetting occurs if:

$$\frac{L}{\Delta S} \geq \frac{2}{1 - \cos \beta} \quad (2)$$

$$\cos \beta = \frac{E_{SV} - E_{LS}}{E_{LV}}$$

where β is the contact angle of the liquid on the hydrophobic surface. From formula (2), Dewetting is favoured for hydrophobic surfaces with a large contact angle, such as FDTS. The simple model suggests that for a given dimension of the hydrophobic stripe, dewetting occurs if the thickness of the film is reduced below a critical thickness (ΔS decreases with decreasing H). This is consistent with detailed modeling of the equilibrium shape of liquid droplets on heterogeneous surfaces⁹, as well as kinetic modeling of dewetting induced by a spinodal instability¹⁰.

In the experiment water is continuously evaporating during the drying process, the concentration of PEDOT/PSS, and thereby the solution viscosity is increasing. If during the drying process the viscosity exceeds a critical value $\eta_{critical}$ before the film

reaches its critical thickness $H_{critical}$ for dewetting, the droplet cannot split completely on top of the hydrophobic lines. This simple model provides an explanation for the experimental observations described above. Since the thickness of the droplet is decreasing from center to edge, dewetting occurs more easily when the hydrophobic line is located near the edge of the droplet. This is also the reason why under certain conditions (Fig 4 a, g) dewetting starts from the thin edge of the droplet, but stops before reaching the thicker center of the droplet. On very hydrophilic surfaces, the more pronounced spreading of the droplet leads to a decrease of its thickness above the hydrophobic strip. Finally, for higher concentration inks, the critical viscosity is reached at larger liquid thicknesses, whereas a low concentration ink is able to dry to a thinner film before it reaches $\eta_{critical}$.

Within the model the beneficial effect of a 30-80 nm thick mesa surface energy barrier on the dewetting process can also be understood. The effect of the mesa is to decrease the liquid film thickness on top of the hydrophobic stripe. When by water evaporation the liquid film thickness decreases to a value comparable to the mesa height, this reduction in effective thickness promotes the dewetting process. Therefore, a solute-containing ink starts to dewet on a mesa-shaped barrier at an earlier time during the drying process, i.e. at a lower viscosity, compared to a monolayer barrier. Dewetting is the easier to achieve, the larger the thickness of the mesa barrier (see Fig. 4 g, h).

The use of a hydrophilic mesa has another important advantage for using split conducting polymer ink droplets as source-drain electrodes of FET devices. Fig. 6a, b and fig. 6e show AFM topography, phase and cross-sectional images, respectively, of dewetted 1:3 PEDOT/PSS droplets split on top of a 250 nm FDTS SAM without mesa. Fig. 6c, d and f give the corresponding dewetting results of 1:1 PEDOT/PSS droplets on a 500 nm wide FDTS SAM with 30 nm mesa. It is seen in Fig. 6a, b and e that the PEDOT/PSS contact line is not in contact with the edge of the FDTS line, and the distance between the contact lines of the two split halves of the PEDOT droplets is significantly larger (about 500 nm) than the width of the FDTS line (250nm). This implies that after dewetting from the FDTS line the contact line of the liquid PEDOT droplets move away from the FDTS line, before it becomes pinned on the substrate.

In contrast, in the case of the mesa structure (Fig. 6c, d and f), the PEDOT/PSS contact line remains pinned to the edge of the mesa structure, and the thickness of the PEDOT/PSS deposit immediately next to the mesa barrier is finite. This can be clearly seen also in Fig. 6f comparing the height of the mesa in the PEDOT free regions (30 nm, red line) of the substrate with the height in the region of the split droplets (25 nm, black line). We believe that this is caused by the wetting nature of the hydrophilic side walls of the SiO₂ mesa which are not modified by FDTS causing the contact line of the drying PEDOT/PSS droplets to remain pinned, leaving channel length accurately defined by the mesa length. In the case of the mesa structure the PEDOT/PSS thickness profile in the vicinity of the surface energy barrier leads to a shorter FET channel length and smaller source-drain contact resistance than in the case of monolayer SAM barriers. The contact resistance is related to the finite conductivity of the PEDOT/PSS, and is minimized by thicker PEDOT films in the vicinity of the injecting source / drain edges. In the case of monolayer FDTS SAMs the channel length tends to be larger, contact resistance is higher, and lower solution concentration need to be used to achieve dewetting which further increases contact resistance. The use of a mesa structure for dewetting is crucial in achieving short submicrometer channel devices by surface energy assisted inkjet printing. By increasing the mesa height the thickness of PEDOT/PSS can be increased, and contact resistance can be lowered (see Fig.4h by comparing the two PEDOT/PSS lines printed with different speed).

The most important role of the mesa for dewetting is that automatically mesa-structure described above is formed. Thereby, dewetting might has potential application in future polymer electronics.

Since the switching speed of a transistor (with a fixed gate line width) is proportional to μ/L , transistors with sub-micrometer channel length and close mobility result in significantly higher switching speed than corresponding micrometer scale devices. Furthermore, submicrometer scale devices offer the possibility of probing the charge transport properties of polymer semiconductors on the length scale of the persistence length of the polymer chains, and the size of microcrystalline domains, which is reported to be on the order of 50 to 100 nm^{19,20,21}. At present, only a few methods have been demonstrated to achieve sub-micrometer channel length, and inorganic

noble metals were employed as electrodes in these reported techniques^{22, 23, 24, 25, 26}. A few methods have been reported to pattern polymer source and drain electrodes^{27, 28, 29, 30}, but sub-micrometer scale channel length can not be defined by these techniques. The present proof-of-concept study shows that the method of surface energy assisted inkjet printing provides sufficient control over the flow of liquid ink droplets to define submicrometer critical features. Of course, EBL might not be the technique of choice for low-cost production of surface energy patterns, but alternative techniques such as direct laser patterning, soft lithographic stamping or embossing might be employed.

An interesting question is whether simple dip coating, rather than inkjet printing, in combination with surface energy patterning can also be used for high resolution patterning of functional inks. For the process of dewetting, inkjet printing and dip-coating (or spin coating) play a similar role of simply delivering liquids to the substrate surface. The virtue of inkjet printing is its ability of putting accurate amounts of liquid to designed positions on the substrate. But in the case of dip coating or spin coating, the same effect can be realized by patterning the substrate surface into small hydrophilic areas where liquids are designed to occupy and hydrophobic areas where liquids are designed not to occupy. Fig. 4f shows a photograph of a photolithographically patterned $\text{SiO}_2/\text{n}^+\text{-Si}$ substrate dip-coated with 1:3 PEDOT/PSS solution. The substrate contains arrays of two rectangular hydrophilic areas separated along one side by a narrow $5\text{ }\mu\text{m}$ hydrophobic FDTS SAM barrier and bound on the other three sides by wide hydrophobic FDTS SAM regions. In this dip-coating (or spin-coating) process, dewetting occurs as a two-step process. In the first step the liquid dewets onto the two hydrophobic regions while still covering the narrow channel in between. Then in a second step the liquid dewets from the narrow channel region. This process happens very much in the same way as described above, provided that the two hydrophilic regions are sufficiently small that the amount of confined liquid is comparable to the liquid deposited in the inkjet case. To facilitate dewetting, the size of the two hydrophilic surface regions needs to be sufficiently small, that the amount of confined liquid is small enough to be able to dewet from the narrow channel region before the solution viscosity reaches its critical value. By careful design of the size of the hydrophilic surface regions, which determines the amount of confined liquid, and adjustment of the solution concentration, the process

of dip coating is capable of achieving similar resolution as the inkjet process described above.

In conclusion, we designed a new transistor structure to decrease off current of short channel transistors. Transistor performance is greatly improved by simply inserting a insulating mesa between source and drain electrodes. This provides a new device architecture to fabricate short channel transistor with good ON-OFF current switching ratio and enhanced performance for application in faster speed integrated circuits.

The processes and devices described herein are not limited to devices fabricated with solution-processed polymers. Some of the conducting electrodes of the TFT and/or the interconnects in a circuit or display device (see below) may be formed from inorganic conductors, that are able to, for example, be deposited by the printing of a colloidal suspension or by electroplating onto a pre-patterned substrate. In devices where not all of the layers deposited from solution, one or more PEDOT/PSS portions of the device may be replaced with an insoluble conductive material such as a vacuum-deposited conductor.

Possible materials that may be used for the semiconducting layer, includes any solution processible conjugated polymeric or oligomeric material that exhibits adequate field-effect mobilities exceeding $10^{-3} \text{ cm}^2/\text{Vs}$ and preferably exceeding $10^{-2} \text{ cm}^2/\text{Vs}$. Materials that may be suitable have been previously reviewed, for example in Ref. 31. Other possibilities include small conjugated molecules with solubilising side chains (32), semiconducting organic-inorganic hybrid materials self-assembled from solution (33), or solution-deposited inorganic semiconductors such as CdSe nanoparticles (34) or inorganic nanowires.

The electrodes may be coarse-patterned by techniques other than inkjet printing. Suitable techniques include soft lithographic printing (35), screen printing (36), and photolithographic patterning (see WO 99/10939), offset printing, flexographic printing or other graphic arts printing techniques. However, ink-jet printing is considered to be particularly suitable for large area patterning with good registration, in particular for flexible plastic substrates. In the case of surface-energy direct deposition, materials may also be deposited by continuous film coating techniques

such as spin, blade or dip coating, which are then able to be self-patterned by the surface energy pattern.

Although preferably all layers and components of the device and circuit are deposited and patterned by solution processing and printing techniques, one or more components may also be deposited by vacuum deposition techniques and/or patterned by photolithographic processes.

Devices such as TFTs fabricated as described above may be part of more complex circuits or devices, in which one or more such devices can be integrated with each other and/or with other devices. Examples of applications include logic circuits and active matrix circuitry for a display or a memory device, or a user-defined gate array circuit.

The present invention is not limited to the foregoing examples. Aspects of the present invention include all novel and inventive aspects of the concepts described herein and all novel and inventive combinations of the features described herein.

The applicant hereby discloses in isolation each individual feature described herein and any combination of two or more such features, to the extent that such features or combinations are capable of being carried out based on the present specification as a whole in light of the common general knowledge of a person skilled in the art, irrespective of whether such features or combinations of features solve any problems disclosed herein, and without limitation to the scope of the claims. The applicant indicates that aspects of the present invention may consist of any such individual feature or combination of features. In view of the foregoing description it will be evident to a person skilled in the art that various modifications may be made within the scope of the invention.

References

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Abstract

Short-channel transistors

An electronic switching device comprising a source electrode, a drain electrode, an insulating layer in the region between source and drain electrode, a semiconducting layer in contact with both the source and the drain electrode, and in contact with said insulating layer, wherein the smallest distance between said source and drain electrodes is less than 1 μm , and wherein the shape of the insulating layer is such that the path of smallest distance between the source-and drain electrodes intersects through a region of said insulating layer, so as to reduce the OFF current of the electronic switching device.

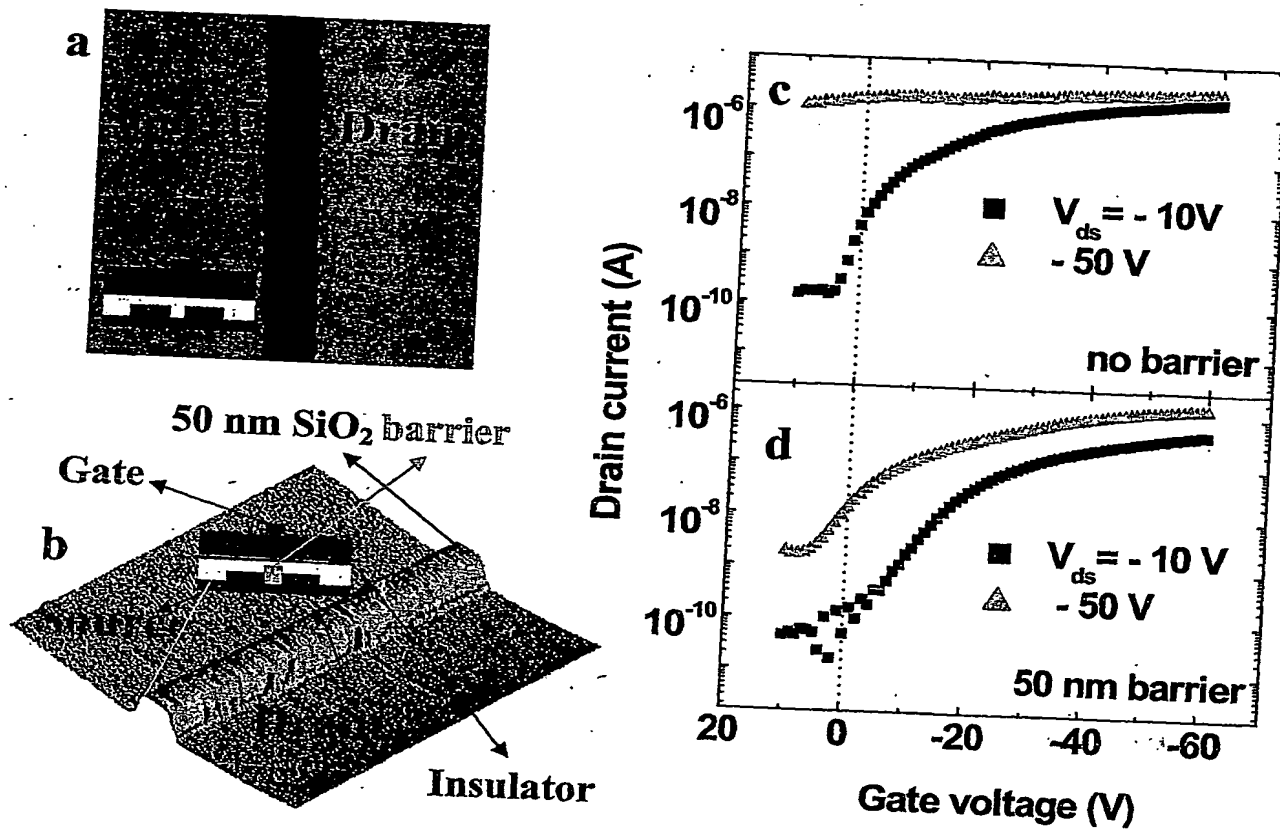
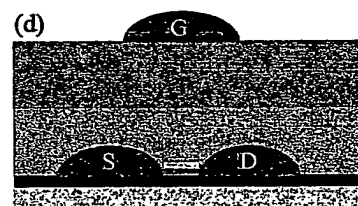
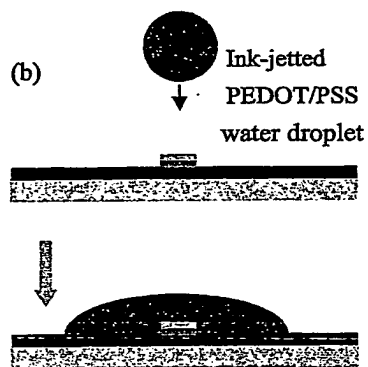







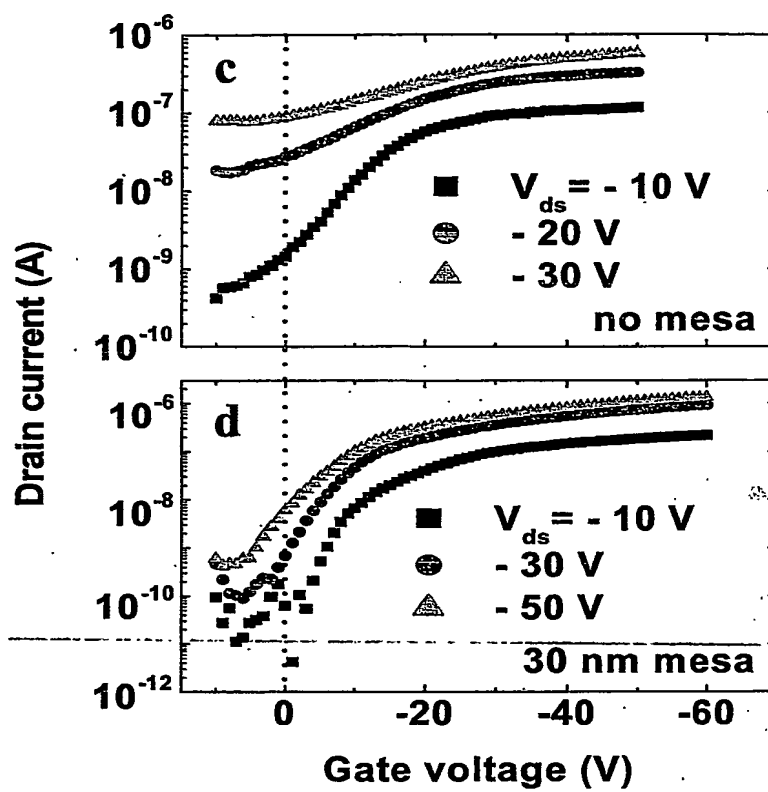
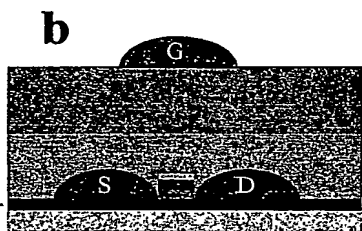
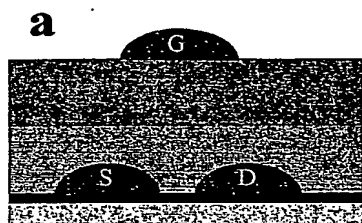
Fig. 1



-  $\text{SiO}_2 / \text{n}^+ \text{-Si}$ substrate
-  evaporated SiO_2
-  FDTs SAM
-  semiconductor layer F8T2
-  insulator layer PMMA

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Fig. 2



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Fig. 3

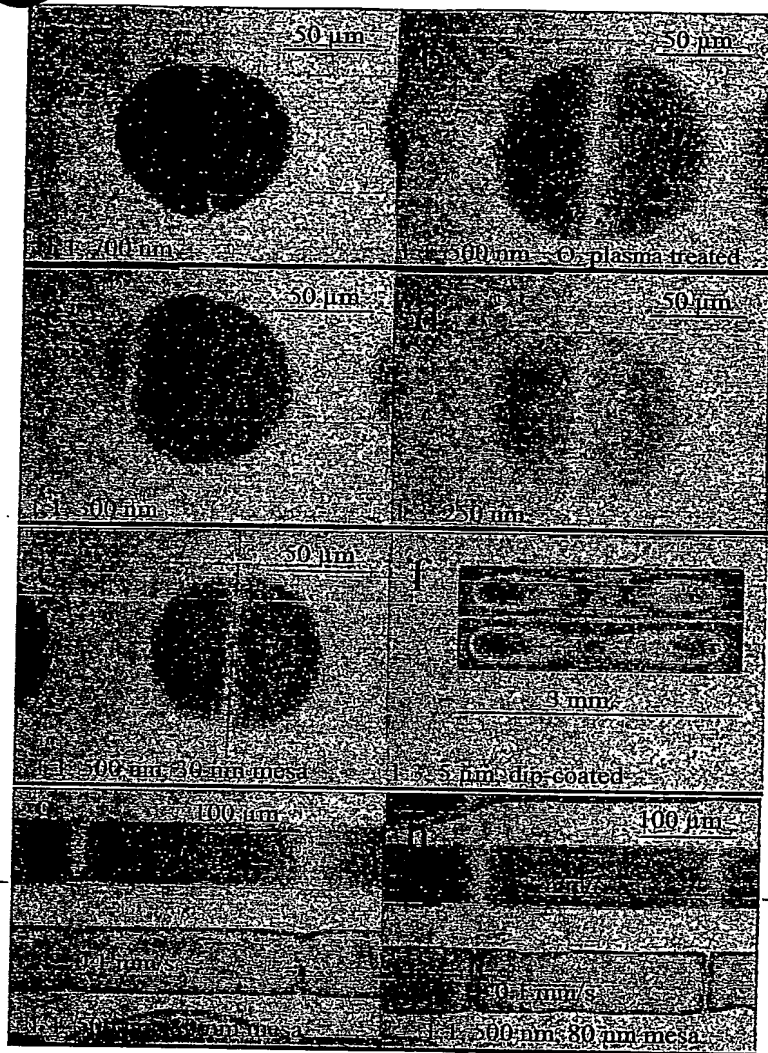


Fig. 4

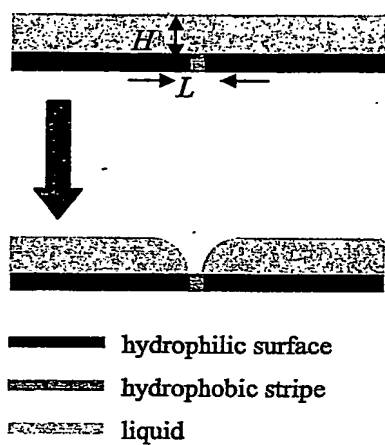


Fig. 5

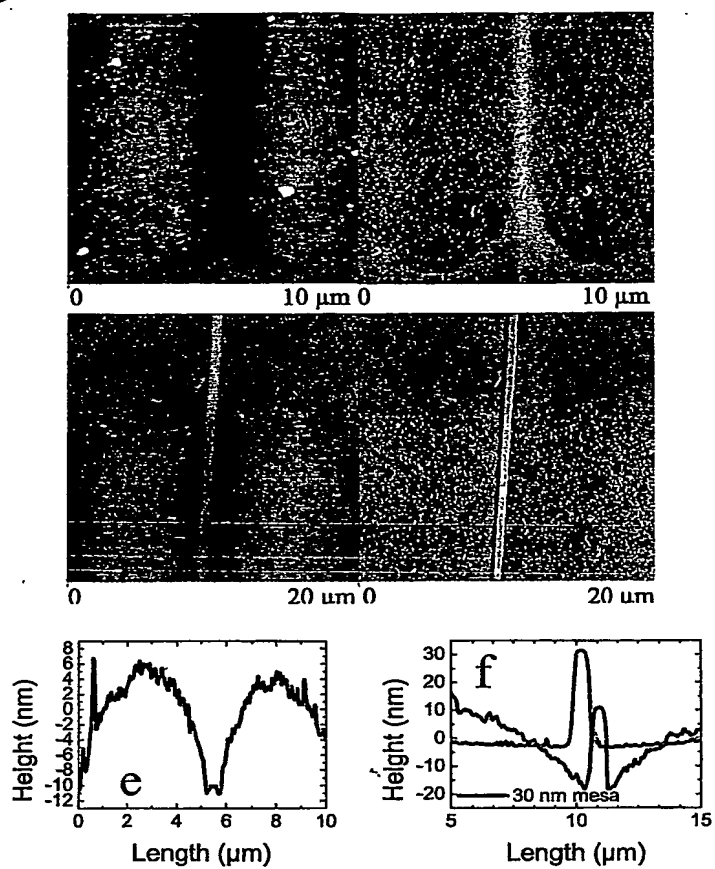


Fig. 6

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